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XA-9472
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Yasuhisa SHIMAZAKI et al.

Appln. No.: 09/855,660 Group Art Unit: 2819

Filed: May 16, 2001 Examiner: D. Chang

For: SEMICONDUCTOR INTEGRATED CIRCUIT HAVING HIGH-SPEED AND LOW-POWER LOGIC GATES WITH COMMON TRANSISTOR SUBSTRATE POTENTIALS, AND DESIGN DATA RECORDING MEDIUM THEREFOR

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

Pursuant to 37 C.F.R. § 1.56, and without any assertion as to materiality or prior art effect, the document listed on the attached Form PTO-1449 is hereby cited.

Respectfully submitted,

By: _____
Mitchell W. Shapiro
Reg. No. 31,568

MWS:sjk

Miles & Stockbridge P.C.
1751 Pinnacle Drive, Suite 500
McLean, Virginia 22102-3833
(703) 903-9000

February 18, 2003